

## Who can Attend it

Faculty Member, Research Scholar, Student and Technical Assistant from Engineering Institutes or Engineer from Industries with Computer Science/ Electronics & Comm./ IT/ Electrical/ Computer Application background.

## Registration

### Registration Fees:

- **Faculty / Research Scholar / Industry Person:** Rs. 1000/-
- **Student:** Rs. 500/-
- **Technical Assistant:** Rs. 500/-

Participants are requested to pay registration fees by cash only. Registration fees need to be submitted at ECE Department of Narula Institute of Technology within 18th June, 2015. Outside candidate (on request) may submit registration fees on 29th June, 2015 at workshop registration desk.

**\* It is to be noted that registration fees excludes fooding / lodging.**

## Mode of Selection

Participants are requested to register for the workshop by filling up an online registration form by [clicking here](#). Application will be accepted on a first come first serve basis. Number of participants is limited to 60.

## Important Dates

**Last date for registration:** 18th June, 2015

**Intimation to applicants:** 28th June, 2015

## Contact Person

- **Mr. Surajit Bari** Ph. No: 9432128450
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### Chief Patron:

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### Coordinator:

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- Mr. Soumen Pal, Asst. Prof. , ECE Dept. , NIT

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- Mrs. Moupali Roy , Asst. Prof. , ECE Dept. ,NIT



## Workshop

On

## Microelectronics & VLSI Design using Advanced Simulation Tools

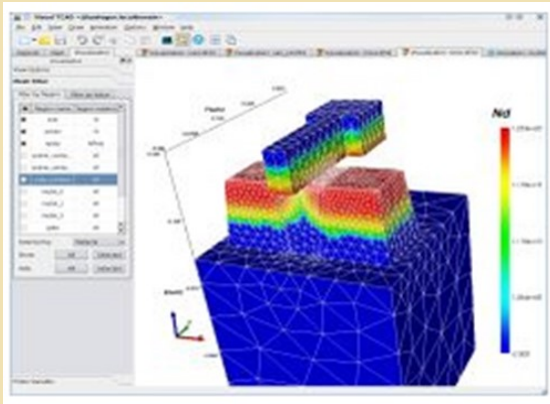
29th June - 10th July 2015

Organized by

ECE Department

Narula Institute of Technology

Agarpara, Kolkata-700109



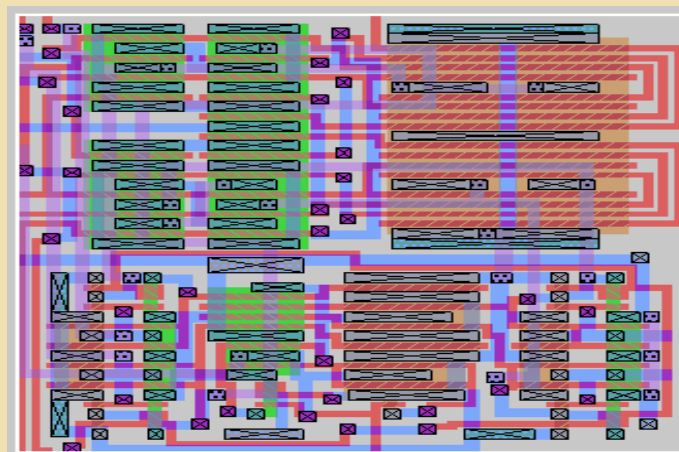
## About the Department

The department of ECE offers premier professional technical training that keeps in pace with the latest developments in the field of Electronics and Communication Engineering. We have excellent infrastructure, highly experienced faculties and professionals, associated with research work which collectively ensure dynamic and vibrant environment in the campus. Some of the Faculty members of this department went to attend International Conferences in abroad. The department organized so many International & National Educational Programs (i.e. IEEE sponsored Seminars, Workshops, Faculty Development Programs and one day educational Industrial tours). There are so many events like Paper presentation, Poster presentation, Technical Quiz contest, Technical Report writing Contest & Technical Workshop cum contest associated with IIT, Bombay are organized for the students by this department. Department has established a student chapter of IETE and it is running successfully. There are more than 150 publications are done by the faculty & students in National & International Journals & Conferences. Furthermore three MODROB Projects funded by AICTE are going on in this department. Many of our Alumni are settled in abroad and also many of the students are GATE qualified and placed in so many reputed Govt. sectors and Private Sectors

Company and Research Organizations. There is also separate Departmental Library apart from the Central Library in the ECE department. There are so many high valued simulation software are present in our department like Tanner SPICE, CADENCE, Matlab, Visual TCAD, HFSS, Qualnet, Active HDL, MPLS, Altera & Xilinx ISE, TMS Kit with Code Composer Studio etc. We have very prestigious PCB design Laboratory with full set up.

## Course Objective

The workshop intends to provide opportunities to faculty member, research scholar, technical assistant as-well-as students to enrich their intellectual validity and further their professional growth. The major focus of the workshop is for the upgradation of outcome based teaching & learning skills and research for the participants in the field of Micro & Nano electronic devices and also for VLSI design in nanoscale using advanced simulation tools. Hands-on exposure to Modern VLSI design and analysis tools like Cadence Virtuoso, Visual TCAD, TSPICE will also be offered to blend the research with implementation for real life problem. Moreover this workshop aims to inculcate learning values in students and monitoring their progress in career.



## Workshop Coverage

- ◇ Basic of MOSFET and Issues to design CMOS circuit
- ◇ Basics of fabrication for Integrated Circuit
- ◇ Advanced Nanoscale Devices
- ◇ HEMT and Advanced MOSFET
- ◇ Quantum Cellular Automata
- ◇ Solar Cell basic to advanced
- ◇ Advanced low power VLSI design
- ◇ High Frequency Devices
- ◇ Training on Cadence Virtuoso
- ◇ Training on Visual TCAD
- ◇ Training on FPGA based system design using Verilog

## Resource Person

- ◆ Prof.(Dr.) C.K.Sarkar, JU
- ◆ Prof.(Dr.) Debashis De, WBUT
- ◆ Prof.(Dr.) H. Saha, IEST, Shibpur
- ◆ Prof.(Dr.) S. Sanyal, JU
- ◆ Prof.(Dr.) Angsuman Sarkar, KGEC.
- ◆ Prof. (Dr.) M. R. Kanjilal, NiT Agarpara
- ◆ Dr. Saradindu Panda, NiT Agarpara
- ◆ Mr. Surajit Bari, NiT Agarpara
- ◆ Lab Session by the experts of Entuple Technologies and Cadre Design Systems
- ◆ Lab Session by Mr. Soumen Pal, NiT Agarpara
- ◆ Lab Session by Mr. Sohan Ghorai, NiT Agarpara

## **Workshop on "Microelectronics and VLSI Design using advanced simulation Tools"**

### **Program Schedule**

Day	Date	Time	Schedule
Day-1	29/06/2015	9:30 AM – 10:30 AM	Registration
		10:30 AM – 11:00 PM	Inaugural Session
		11:00 AM – 1:00 PM	HEMT and Advanced MOSFET [Prof.(Dr.) C. K. Sarkar, JU]
		1:00 PM – 2:00 PM	Lunch Time
		2:00 PM – 4:00 PM	Basics of MOSFET & issues to design CMOS Circuit [Mr. Surajit Bari, NiT Agarpara]
Day-2	30/06/2015	11:00 AM – 1:00 PM	Quantum Cellular Automata [Prof.(Dr.) Debashis De, WBUT]
		1:00 PM – 2:00 PM	Lunch Time
		2:00 PM – 4:00 PM	FPGA based system design using Verilog [Sohan Ghorai, NiT Agarpara]
Day-3	01/07/2015	11:00 AM – 1:00 PM	Basics of fabrication for integrated Circuits [Dr. Saradindu Panda, NiT Agarpara]
		1:00 PM – 2:00 PM	Lunch Time
		2:00 PM – 4:00 PM	FPGA based system design using Verilog [Sohan Ghorai, NiT Agarpara]
Day-4	02/07/2015	11:00 AM – 1:00 PM	Solar Cell - Basic to Advance [Prof.(Dr.) H. Saha, IEST Shibpur]]
		1:00 PM – 2:00 PM	Lunch Time
		2:00 PM – 4:00 PM	FPGA based system design using Verilog [Sohan Ghorai, NiT Agarpara]
Day-5	03/07/2015	11:00 AM – 1:00 PM	Advanced low power VLSI Design [Prof.(Dr.) S. Sanyal, JU]
		1:00 PM – 2:00 PM	Lunch Time
		2:00 PM – 4:00 PM	FPGA based system design using Verilog [Sohan Ghorai, NiT Agarpara]
Day-6	06/07/2015	11:00 AM – 1:00 PM	Training on Cadence [Entuple Technologies]
		1:00 PM – 2:00 PM	Lunch Time
		2:00 PM – 4:00 PM	Training on Cadence [Entuple Technologies]
Day-7	07/07/2015	11:00 AM – 1:00 PM	Training on Cadence [Entuple Technologies]
		1:00 PM – 2:00 PM	Lunch Time
		2:00 PM – 4:00 PM	Training on Cadence [Entuple Technologies]
Day-8	08/07/2015	11:00 AM – 1:00 PM	Training on Cadence [Entuple Technologies]
		1:00 PM – 2:00 PM	Lunch Time
		2:00 PM – 4:00 PM	VLSI Design using Cadence Tools [Mr. Soumen Pal, NiT Agarpara]

Day-9	09/07/2015	11:00 AM – 1:00 PM	Training on TCAD [Cadre Design Systems]
		1:00 PM – 2:00 PM	Lunch Time
		2:00 PM – 4:00 PM	Training on TCAD [Cadre Design Systems]
Day-10	10/07/2015	11:00 AM – 1:00 PM	Nano Scale Devices [Prof.(Dr.) Angsuman Sarkar, KGEC]
		1:00 PM – 2:00 PM	Lunch Time
		2:00 PM – 3:30 PM	High Frequency Devices [Prof. (Dr.) M. R. Kanjilal, NiT Agarpara]
		3:30 AM – 4:30 PM	Valedictory Session