NARULA INSTITUTE OF TECHNOLOGY
81, Nilgunj Road, Agarpara, Kolkata- 700109

REPORT ON
Short Term Course

1. **Name of the Participant :** SOHAN GHORAI

2. **Department :** ECE **3. Designation:** Assistant Professor

4. **Category :** [√] Faculty [ ] TA [ ] ther Staff

5. **Sponsorship :** [√] NIT [ ] Self

6. Title of the Seminar : **TEQIP-II Short Term Course on FDP for Effective Teaching From the 17th to the 19th of July 2014**

7. **Seminar Organized by :** Centre for Educational Technology, IITKGP

8. **Duration:** 3 days (17th to 19th July 2014). **Total Participant:** 50

10. **Topic Discussed :**

1. Outcome Based Learning, Washington Accord, NBA guideline.
2. Taxonomies and Instructional Objectives.
3. Assessment and Evaluation
4. Outcome based Curriculum Design and Software
5. Supervised Practice session for Outcome based Curriculum Design and Software
6. Artificial Intelligence in Education
7. What is good teaching and its Attributes.
8. Introduction & Demonstration to the MOODLE software
9. Communication and presentation Skills.
10. Research Methodology.

11. **Name of the speakers (with Contact Nos. ,if possible):**
Prof Bani Bhattacharya,
Dr. Shyamal Das Mandal,
Prof.A.K.Ray,
Prof S.K.Som,
Dr.Tamali Bhattacharya,
Dr. P.K.Bhowmik

12. **Name of the Other Participating Institutes:**
    1. RCC
    2. MCKV
    3. BUIE, Bankura.
    4. CEMK, Kolaghat

13. Brief report on the deliberation of the Seminar (to be attached as Annexure-1):

14. Presentation given at NIT on ___any Suitable Date.

15. Presentation Attended by : [√] Faculty Students [ ]

.....

Date : Signature of the Participant

Comments By HOD (with special emphasis on how NIT has been benefited) :

.....

Signature of HOD

....

Signature of Principal Signature of Director

ANNEXURE-1

IIT,KGP conducted a Short Term Course on FDP for Effective Teaching From 17thJuly to 19th July,2014 at CET building, IIT Campus. Prof.A.K.Ray & Dr.S.K.Das Mandal co-ordinate the entire program and the overall program is very satisfactory & learner-centric.

On the day beginning after introduction , some aspects of Artificial Intelligence such as knowledge representation, reasoning under uncertainty, planning, goal recognition, virtual learning environment (MOODLE) ,attributes of good teaching etc are discussed .The program starts at 9.00 am & ends at 6.30 pm. The lectures are given by Dr. P.K. Bhowmik, Mr.S.Nayak, Prof.A.K.Ray & Prof S.K.Som
Dr. P.K.Bhowmik.
Topics covered on the 2nd day are Washington Accord Graduate attribute, knowledge of engineering & science, design/development of solutions, modern tool usage, project management, course level matrix, program level matrix Bloom's taxonomy, Domain of learning, Instructional objectives & Practice session of Outcome based curriculum. The lectures are given by Prof.A.K.Ray, Prof.Bani Bhattacharya & Dr.S.K.Das Mandal. The same scheduled time is maintained.

On the last day of discussion, Course Objective, Module Objective & Unit Objective, action verb, Nature of presentation, Terminal objectives, Time & other constraints, Research Methodology are communicated. The lectures are given by Prof.A.K.Ray,Prof.Bani Bhattacharya , Dr.S.K.Das Mandal & Dr.Tamali Bhattacharya. After completion of the lecture certificates are distributed to the learner.

Report

On

Advanced Faculty Training at C-DAC, Kolkata

Date: 05/02/2013

Prof. (Dr.) M.R.Kanjilal

Head, ECE department

Narula Institute of Technology

81, Nilgunj Road, Agarpara, Kolkata-700109

Respected Madam,

In keeping with my undertaking agreement regarding past faculty development program visit at C-DAC , I am submitting the accompanying background report entitled Report on Advanced Faculty Training at C-DAC, Kolkata.

The purpose of the report is to share my experience, knowledge and outcome of that visit. In addition, the report discusses about the topics and hands-on provided in the training. The report concludes with a review of how my visit can enrich institutional development program.

Hope this report will prove to be satisfactory.

Respectfully Yours,

SohanGhorai

Assistant Professor

ECE Department

Narula Institute of Technology

Report on Advanced Faculty Training at C-DAC, Kolkata

Objective: To gain and share some knowledge on Advanced Digital Signal Processing, Speech and Image Processing.

Experience: Advanced Faculty Training on Digital Signal Processing, Speech and Image Processing is an academia knowledge sharing initiative taken by Centre for Development of Advanced Computing (C-DAC), Kolkata. The training was a two weak full time course from 31st December 2012 to 11th January 2013. The primary objective of this programmeis to update/enhance the skills of engineering faculties in advanced domains of Information Technology keeping pacewith the IT industry. The engineering faculties may be exposed to the needs of IT industry so that they can in-turn nurture, educate and mould their students while they are still in the college.

The training methodology includes:

- State-of-the-art course wire
- Module wise case studies
- Matlab based laboratory assignment
- Classroom Lectures
- Special lecture session by external experts

Each module they had prepared for delivery, aimed for practical aspect of that theory and some of which related to their current research work. The content they have covered have been listed below:

Digital Signal Processing:

1. Overview of DSP
2. Signal & Systems
3. Fourier Series, z-Transform, Wavelet Transform
4. Different digital filters and their application
5. Recent research trends in DSP including their work

Speech Processing:

1. Introduction of Speech Signal Processing
2. Knowledge sources in speech like time and frequency domain, spectrograms etc.
3. Modelling techniques for developing speech system like VQ, HMM, GMM etc.
4. Speech recognition
5. Speech synthesis
6. Speaker recognition

Image processing:

1. Basic image processing
2. Frequency domain analysis of signal – Fourier to wavelets
3. Image compression and different formats
4. Video tracking and processing
5. Introduction to pattern in Image Processing
6. Feature extraction
7. Classification and Clustering
8. Laboratory experiments of the above mentioned algorithms

Mr. Milton SamirakshmaBepari of CDAC, Kolkata given an introduction on DSP and its application in image processing. Practical session in this module includes some basic filter design in MATLAB. Dr.Y.K.Sing of CDAC, Bangalore, has discussed some advances in transformation technique in signal processing and a linked hands-on session have been made on advanced filter like optimal filter,

comb filter etc. we have learned some application of scientific computing on embedded platform like e-Agri instrument, e-nose, image acquisition hardware development. Mr.DebasisMazumdar of CDAC, Kolkata, has discussed some of the limitations of existing mathematics used in DSP and introduction to stastical signal processing. Prof.P.K.Das from IIT Guwahati conducted a special session on speech processing , speech production model and feature extraction. Some practical case studies and hands-on session made on Speech synthesis and Speaker Recognition. In contrast to that knowledge, some interesting research affairs discussed by Prof Ashoke Kumar Dutta from ISI on "Cognition and its application in speech synthesis". Throughout that discussion, some research problem has been thrown to us, which will add some value in my research progress. Prof.T.K.Basu of IIT, Kharagpur given lectures on image processing. We have gone through some hands-on session on designing an algorithm for image compression using MATLAB. They have discussed some research problems on "Machine Vision" and "Vision Perception Engineering". We have also gone through some of the case studies like:

1. Fingerprint Verification
2. Bullet Cartridge Identification
3. Face Recognition
4. Facial Expression Analysis
5. Quality testing of Tea Leaf
6. Character Recognition Software Development

Beside normal course module, an awareness session conducted on "Cyber Security and Rules" for the software developers working in this area. I want to thank Mr.SantanuRanjanDutta for supplying necessary documents, books, website links and research materials.

Outcomes: I have gained extensive details of subject knowledge along with practical knowledge. Case studies and practical examples enrich my concept on that topic and that will help me to conduct lab in my institution. The research problems they have thrown, also help me in my research activity and also for my students.

Institutional

Development: What I can contribute for the institute has been listed below:

- I can share my knowledge among the students.
- Practical ideas gained during that training will be helpful for performing innovative experiment in lab session.
- I can share the tutorial material among students provided by CDAC.
- I can help to add extra tutorials in the curriculum of UG and PG course to meet industrial needs.
- UG and PG students can be motivated in research work by providing small research problems as a project.
- I can help to arrange some collaborative R&D activity in our institution for upliftment of our research activity.

Report

On

Workshop on Xilinx FPGA Architecture and Design Flow at IIT Guwahati, Assam

Date: 12/11/2013

Prof. (Dr.) M.R.Kanjilal

Head, ECE department

Narula Institute of Technology

81, Nilgunj Road, Agarpara, Kolkata-700109

Respected Madam,

In keeping with my undertaking agreement regarding past faculty development program visit at IIT Guwahati, I am submitting the accompanying background report entitled Report on Xilinx FPGA Architecture & Design Flow at IIT Guwahati, Assam.

The purpose of the report is to share my experience, knowledge and outcome of that visit. In addition, the report discusses about the topics and hands-on provided in the training. The report concludes with a review of how my visit can enrich institutional development program.

Hope this report will prove to be satisfactory.

Respectfully Yours,

Sohan Ghorai

Assistant Professor

ECE Department

Narula Institute of Technology

Report on Xilinx FPGA Architecture & Design Flow at IIT Guwahati, Guwahati, Assam

Objective: To gain and share some practical knowledge on Xilinx FPGA architecture and hardware development on Xilinx FPGA development board.

Experience: Workshop on Xilinx FPGA Architecture & design Flow is an academia knowledge sharing initiative taken by Xilinx university program and IIT Guwahati. The training was a two days full time course from 22nd November 2013 to 23rd November 2013. The primary objective of this programmeis to train academician and researcher to handle latest development kit developed by Xilinx and familiarisation of their latest development tools.

The training methodology includes:

- State-of-the-art course wire
- Latest development kit
- Vivado tool based laboratory assignment
- Video tutorials
- Special lecture session by external experts

Each tool present in Xilinx ISE development suit had been clearly demonstrated by experts from Xilinx. The content they have covered have been listed below:

Xilinx FPGA Development Tools:

6. FPGA architecture and design flow
7. Development examples with Xilinx ISE and Verilog
8. Implementation of ILA and VIO in FPGA and testing using Chipscope Pro
9. Plan Ahead based Flow
10. Xilinx ISE design flow and hardware implementation
11. Xilinx Embedded Design flow using Platform Studio
12. Matlab integration with Xilinx DSP design flow using system generator for DSP
13. Hardware Software co-simulation
14. Zynq architecture and embedded design flow using ZedBoard
15. Overview of Vivado HLS

Workshop started with an inauguration ceremony and address by director IIT Guwahati, guest-of-honour, deputy director and Head-EEE department. Xilinx India university program manager Mr.Samik Biswas address the scope and opportunity of this initiative from Xilinx. Their after Mr. V Damodora presented Xilinx FPGA architecture and design flow. Example project using Altys 3 development board demonstrated by Mr.Satyabrata Das. Concepts on chip debugging using Xilinx Chipscope Pro was demonstrated by Mr. V Damodora. Concept of chip debugging using ILA and VIO IP core was very interesting. We have gone through Plan Ahead based flow and implementation using Altys 3 board. Mr. V Damodora demonstrated Xilinx embedded design flow using XPS and SDK, concepts of hardware modelling – use of Matlab and Simulink and integrating with Xilinx DSP design flow using system generator for DSP. On next day, we have gone through system modelling and HDL generation using system generator, Xilinx DSP design flow and concepts of hardware co-simulation. Last part of this session given a demonstration on Zynq architecture and embedded design flow using Zed Board and Vivado HLS design flow.

I want to thank Dr.Gourav Trivedi for supplying necessary documents, books, website links and research materials.

Outcomes: I have gained extensive details of subject knowledge along with practical knowledge. Case studies and practical examples enrich my concept on that topic and that will help me to conduct lab in my institution. The research problems they have thrown, also help me in my research activity and also for my students.

Institutional

Development: What I can contribute for the institute has been listed below:

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- UG and PG students can be motivated in research work by providing small research problems as a project.
- I can help to arrange some collaborative R&D activity in our institution for upliftment of our research activity.